

## U.S. UTILITY Patent Application

O.I.P.E.		PATENT DATE
SCANNED	Q.A.	

APPLICATION NO. 09/880458	CONT/PRIOR D	CLASS <del>710</del>	SUBCLASS	ART UNIT <del>2482</del>	EXAMINER V. TAN
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## APPLICANTS

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326 39+ 2819  
Claimed invention is directed to multicasting.  
Proposed logic circuit interconnections with shroud pins

### TITLE

I/O circuitry shared between processor and programmable logic portions of an integrated circuit

<b>ISSUING CLASSIFICATION</b>									
<b>ORIGINAL</b>				<b>CROSS REFERENCE(S)</b>					
<b>CLASS</b>		<b>SUBCLASS</b>		<b>CLASS</b>	<b>SUBCLASS (ONE SUBCLASS PER BLOCK)</b>				
<b>INTERNATIONAL CLASSIFICATION</b>									

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner) _____ (Date)			<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) _____ (Date)			<b>ISSUE BATCH NUMBER</b>	

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